In the Claims:

Please amend the claims as follows:

A2

1. (Amended) A method for forming a spacer, comprising:

depositing [an] a first oxide layer over [a] at least two polysilicon [line] lines of a core and periphery area;

performing a first spacer etch in the core and periphery area;

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implanting an area located between two polysilicon lines in the core area;

applying a second oxide layer over the core and periphery areas; and

performing a second spacer etch over the periphery area wherein a [difference] different appearance of the core and periphery area is produced.

2. The method of claim 1 wherein the first oxide [deposition] layer has a thickness of less than one-half the distance between a periphery of [the] adjacent polysilicon lines.

3. A [non volatile] non-volatile memory device made by the method of claim 1.

4. A [non volatile] non-volatile memory device made by the method of claim 2.

Please add the following new claims:

5. A process for fabricating a non-volatile memory device comprising:

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providing a substrate having a core area, a periphery area, and at least two polysilicon lines overlying the core area and the periphery area;

depositing a first oxide layer over the polysilicon lines;

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performing a first spacer etch in the core area and the periphery area;

implanting an area located between at least two polysilicon lines in the core area;

depositing a second oxide layer over the core and periphery areas; and

performing a second spacer etch over the periphery area.

6. The process of claim 5, wherein the first oxide layer has a thickness of less than one-half the distance between a periphery of adjacent polysilicon lines.

A3 cont'd

7. The process of claim 5 further comprising performing a second spacer etch over the core area.

8. The process of claim 5, wherein the implanting of an area occurs after the performing of the first spacer etch.

9. The process of claim 5, further comprising implanting an area located between at least two polysilicon lines in the periphery area.

10. The process of claim 9, wherein the implanting of an area located between at least two polysilicon lines in the periphery area occurs after the performing of the first spacer etch.

11. The process of claim 9, wherein the implanting of an area located between at least two polysilicon lines in the core area occurs after the performing of the second spacer etch.

12. A process for making an electronic component comprising:
forming a memory cell by the process of claim 5; and
forming the electronic component comprising the memory cell.

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13. A process for fabricating a memory cell comprising the steps of:
providing a substrate having a core area, a periphery area, at least two polysilicon lines overlying the core area and the periphery area, and first spacers adjacent the at least two polysilicon lines overlying the core area and the periphery area; and
forming a second spacer adjacent at least one first spacer.

14. The process of claim 13, further comprising implanting an area located between at least two polysilicon lines in the core area.